CH-471A

Motherboard

User's Manual

Mainboard Specification

- CPU support
  - INTEL 80486DX/DX2, 80486SX, 80487SX PGA package
    SL enhanced PGA package
    P24T PGA package
    P24C (80486DX4) PGA package
    P24D PGA package
  - AMD AM486DX/DX2/DXL/DX2L PGA package
  - Cyrix CX486S, CX486DX, CX486DX2 PGA package
- Frequency: support system running 25/33/40/50 MHz
- System chipset: SIS 85C471, 85C407
- Cache size: write back direct mapped cache with size of 32/64/128/256KB/512K/1M selection.
- SRAM type: TAG SRAM 8KX8/16KX8/32KX8/64KX8
  DATA SRAM 8KX8/32KX8/64KX8/128KX8.
- DRAM size: four banks up to 128 MB
- DRAM type: support 256K/512K/1M/2M/4M/8M/16M 72 pin SIMM module.
- Slots: seven 16 bit ISA slots, one 8 bit ISA slot, two VESA master mode slots, one SLAVE mode slot, located at ISA slot 1,2,3.
- Dark Green-PC function:
  - Support: HDD standby
    Monitor standby
    CPU stop clock -> INTEL SL enhanced
    Cyrix CX486S/DX/DX2
    CPU slow clock (8 MHz) -> INTEL/AMD 486SX/DX/DX2.
- Support green power supply connector for controlling AC output power and VESA VGA monitor control through VGA feature connector.
- On board adjustable voltage regulator for INTEL 80486DX4(P24C) CPU.
- Hardware power down switch supported.

2 Hardware Description

Connector and Jumper Settings

This chapter describes the main board's jumpers and connectors. For the system layout, please refer to Appendix A.

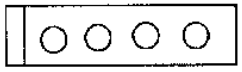
Connectors

J2: Power Supply Connector

J1: Keyboard Connector

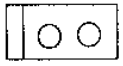
J19:

1-4: Used for external battery connector.



PIN 1 : VDC
PIN 4 : GROUND

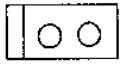
J3: Hardware Reset
Open: Normal **Short: Reset**



RESET

PIN 1 : RESET INPUT
PIN 2 : GROUND

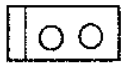
J5: Turbo Switch
Open: Turbo **Short: Normal**



TBSW

PIN 1 : TURBO ACTIVE
PIN 2 : GROUND

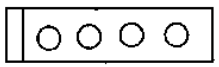
J6: Turbo LED



TBLD

PIN 1 : LED POWER
PIN 2 : LED CATHODE

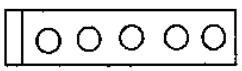
J8: Speaker Connector



SPKR

PIN 1 : DATA OUT
PIN 2 : N. C.
PIN 3 : GROUND
PIN 4 : +5V VDC

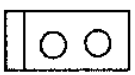
J7: Keylock and Power LED Connector



KBLOCK

PIN 1 : LED POWER
PIN 2 : N. C.
PIN 4 : KEYBOARD INHIBIT
PIN 3,5 : GROUND

J4: Power Saving Switch Connector



Open : Normal
Short : Power down state

NOTE:
When this switch is short, it will force the system to enter power down mode. At the same time the turbo LED will be off to indicate its status.

JP6: Clock down control select.
Always 2-3 short by SMOUT 0 control.

JP38, 39: Green-PC function connector.
Detail description see page 2-12 and 2-13.

CPU Type Selection

Jumpers

A. CPU Clock Selection

JP8, 12, 13: Pin Header 1 x 2

Frequency	JP8	JP12	JP13	CPU Type
20 MHz	OPEN	OPEN	OPEN	486DX/SX-20 CX486S2/DX2-40
25 MHz	OPEN	OPEN	SHORT	486DX/SX-25, 487SX-25 486DX2-50/Cx486DX2-50 Cx486S/DX-25
33 MHz	SHORT	SHORT	SHORT	486DX/SX-33, 487SX-33, P24C 486DX2-66, Cx486DX2-66 Cx486S/DX-33
40 MHz	OPEN	SHORT	SHORT	486DX/SX-40 Cx486S/DX-40
50 MHz	SHORT	OPEN	OPEN	486DX-50 Cx486DX-50

NOTE:
CPU not shown above, please make sure their operation frequency works normally for example: INTEL P24CT series CPU.

B. Cache SRAM Size Selection

JP2,3,4,5,14,16: pin header 1x3
JP1: pin header 1x5

Cache Size	JP1	JP2	JP3	JP4	JP5	JP14	JP16
32K	1-2, 3-4	2-3	1-2	1-2	1-2	1-2	1-2
64K	2-3, 4-5	1-2	1-2	2-3	1-2	1-2	1-2
128K	1-2, 3-4	2-3	2-3	2-3	1-2	1-2	2-3
256K	2-3, 4-5	1-2	2-3	2-3	2-3	1-2	2-3
512K	1-2, 3-4	2-3	2-3	2-3	2-3	2-3	2-3
1M	2-3, 4-5	1-2	2-3	2-3	2-3	2-3	2-3

C. CPU Type Selection

JUMPER / CPU TYPE	JP20	JP21	J29	JP31	JP25	JP23	JP26	JP24	JP11	JP10	JP30	JP33	JP36	JP28	JP27
486SX	2-3	OPEN	2-3	OPEN	OPEN	OPEN	OPEN	OPEN	2-3	1-2	OPEN	OPEN	OPEN	OPEN	OPEN
486DX	1-2	SHORT	2-3	3-4	OPEN	OPEN	OPEN	OPEN	2-3	1-2	OPEN	OPEN	OPEN	OPEN	OPEN
P24T	1-2	SHORT	1-2	2-3	3-4	OPEN	2-3	1-2	1-2	1-2	1-2	1-2	1-2	OPEN	OPEN
SL-ENHANCE 486SX	2-3	OPEN	2-3	OPEN	3-4	1-2	2-3	4-5	2-3	1-2	OPEN	OPEN	1-2	OPEN	OPEN
SL-ENHANCE 486DX2	1-2	SHORT	2-3	3-4	3-4	1-2	2-3	4-5	2-3	1-2	OPEN	OPEN	1-2	OPEN	OPEN
SL-ENHANCE 486DX	1-2	SHORT	2-3	3-4	3-4	1-2	2-3	4-5	2-3	1-2	OPEN	OPEN	1-2	OPEN	OPEN
CYRIX 486S (M6)	2-3	OPEN	2-3	OPEN	2-3, 4-5	OPEN	1-2, 3-4	2-3	1-2	2-3	2-3	2-3	1-2	OPEN	OPEN
CYRIX 486DX/DX2	1-2	SHORT	2-3	3-4	2-3	OPEN	1-2, 3-4	2-3	1-2	2-3	2-3	2-3	1-2	OPEN	OPEN
P24D	1-2	SHORT	1-2	3-4	1-2, 3-4	2-3	2-3	4-5	2-3	1-2	OPEN	OPEN	1-2	SHORT	SHORT
INTEL DX4 (P24C) *	1-2	SHORT	2-3	3-4	3-4	1-2	2-3	4-5	2-3	1-2	OPEN	OPEN	1-2	OPEN	OPEN
~~AM486DXL-DX4~~	~~1-2~~	~~SHORT~~	~~2-3~~	~~1-2~~	~~OPEN~~	~~OPEN~~	~~OPEN~~	~~OPEN~~	~~2-3~~	~~1-2~~	~~3-4~~	~~OPEN~~	~~2-3~~	~~OPEN~~	~~OPEN~~

JP22 : Short for Cx486S2 only

Remarks "*": If CH-471A with regulator is on Q3 or Q4, then it can support 3.3V P24C (486DX4)

D. VESA Local Bus ID Selection

JP44, JP47: Pin Header 1x3

Wait state selection	JP44
High speed 0-wait	1-2 Short
High speed 1-wait	2-3 Short

VL-Bus operation clock	JP47
VESA clock and CPU clock >33 MHz	2-3 Short
VESA clock and CPU clock <=33 MHz	1-2 Short

NOTE:
e.g. 486DX2-50 CPU clock = 25 MHz
486DX2-66 CPU clock = 33 MHz

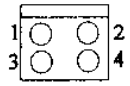
E. CMOS Clear

JP7: Pin Header 1x3
1-2 Short - Normal
2-3 Short - Clear CMOS Data

CAUTION:
Before shorting JP7, first power off the mainboard and should be kept 1-2 short in normal operation.

F. Others

JP37: Regulator voltage selection



JP37

1-2 short: 3.3 V
3-4 short: 3.15 V

JP32,34,35 : CPU power selection (for P24C/P24CT) jumper.
Pin header 3 x 3
1-2 (all) : +5 V voltage
2-3 (all) : +3.3/3.15 V (select the JP37 voltage selection).

SRAM Configuration

Cache size	TAG SRAM size	Data SRAM size	Q'ty	Banks	Cacheable memory range
32KB	8K x 8	8K x 8	4 pcs	1	8MB
64KB	8K x 8	8K x 8	8 pcs	2	16MB
128KB	8K x 8	32K x 8	4 pcs	1	32MB
256KB	16K x 8	32K x 8	8 pcs	2	64MB
512KB	32K x 8	128K x 8	4 pcs	1	128MB
1MB	64K x 8	128K x 8	8 pcs	2	128MB

NOTE:
Locations:
TAG SRAM : U11
Data SRAM : Bank 0 - U1, 3, 5, 7
Bank 1 - U2, 4, 6, 8

Cache Speed Options

The external cache can be configured as non-interleaved or interleaved for two bank SRAM installed, for two-bank interleaved cache can use slower cache DATA SRAMs.

The BIOS support Cache Read Burst timing and write cycles for SRAM setting. The cache read provide four options: 2-1-1-1, 3-1-1-1, 2-2-2-2 and 3-2-2-2, and cache write provide two options: 2T or 3T.

DATA SRAM Specification of speed

Cache Configuration		Interleave	25MHz	33 MHz	40MHz	50MHz
Read 2-1-1-1	Write 2T	Yes	-35ns	-20ns	-12ns	------
Read 2-1-1-1	Write 2T	No	-25ns	-15ns	-----	-----
Read 2-1-1-1	Write 3T	Yes	-40ns	-25ns	-20ns	-----
Read 2-1-1-1	Write 3T	No	-25ns	-15ns	-----	-----
Read 3-1-1-1	Write 3T	Yes	-45ns	-25ns	-20ns	-12ns
Read 3-1-1-1	Write 3T	No	-25ns	-15ns	-----	-----
Read 2-2-2-2	Write 2T	No	-35ns	-20ns	-12ns	-----
Read 2-2-2-2	Write 3T	No	-40ns	-25ns	-20ns	-----
Read 3-2-2-2	Write 3T	No	-65ns	-45ns	-35ns	-25ns
Read 3-2-2-2	Write 3T	Yes	-80ns	-55ns	-45ns	-30ns

TAG SRAM Specification of speed

Cache Configuration		25MHz	33MHz	40MHz	50MHz
Read 2-1-1-1/2-2-2-2	Write 2T	-25ns	-20ns	-12ns	-----
Read 2-1-1-1/2-2-2-2	Write 3T	-25ns	-25ns	-15ns	-----
Read 3-2-2-2	Write 3T	-45ns	-35ns	-25ns	-20ns

DRAM Bank Configuration

DRAM Speed Options

The DRAM socket SIM1, SIM2, SIM3 and SIM4 support single side or double side 72 pin SIMM DRAM module.

The BIOS support 4 read and 2 write speed options. The 4 read options are ***"Fastest", "Faster", "Slower"*** and ***"Slowest"***, and 2 write options are ***0WS*** or ***1WS*** (WS means wait state). The 4 options of DRAM access timing is shown below.

	Fastest 25MHz	Faster 33MHz	Slower 40MHz	Slowest 50MHz
RAS-to-CAS delay	1.5T	2T	2T	3T
Read CAS pulse width	1.5T	2T	3T	3T
RAS percharge	3T	3T	4T	5T
CAS percharge	0.5T	1T	1T	2T

NOTE:
The CAS percharge can be selected in BIOS "DRAM Write CAS" for 1T or 2T.

The following is the configuration table:

Bank 0 (SIM 1)	Bank 1 (SIM 2)	Bank 2 (SIM 3)	Bank 3 (SIM 4)	Total
256K x 36-S				1MB
256K x 36-S	256K x 36-S			2MB
512K x 36-D				2MB
256K x 36-S	256K x 36-S	512K x 36-D		4MB
512K x 36-D	512K x 36-D			4MB
1M x 36-S				4MB
256K x 36-S	1M x 36-S			5MB
256K x 36-S	256K x 36-S	1M x 36-S		6MB
512K x 36-D	1M x 36-S			6MB
256K x 36-S	256K x 36-S	512K x 36-D	1M x 36-S	8MB
512K x 36-D	512K x 36-D	1M x 36-S		8MB
1M x 36-S	1M x 36-S			8MB
2M x 36-D				8MB
256K x 36-S	256K x 36-S	1M x 36-S	1M x 36-S	10MB
256K x 36-S	256K x 36-S	4M x 36-S		18MB
512K x 36-D	512K x 36-D	1M x 36-S	1M x 36-S	12MB
1M x 36-S	1M x 36-S	1M x 36-S		12MB
1M x 36-S	1M x 36-S	1M x 36-S	1M x 36-S	16MB
2M x 36-D	2M x 36-D			16MB
4M x 36-S				16MB
256K x 36-S	4M x 36-S			17MB
512K x 36-D	4M x 36-S			18MB
512K x 36-D	512K x 36-D	4M x 36-S		20MB
1M x 36-S	4M x 36-S			20MB
512K x 36-D	512K x 36-D	1M x 36-S	4M x 36-S	24MB
1M x 36-S	1M x 36-S	4M x 36-S		24MB

2M x 36-D	2M x 36-D	2M x 36-D		24MB
4M x 36-S	4M x 36-S			32MB
2M x 36-D	2M x 36-D	2M x 36-D	2M x 36-D	32MB
8M x 36-D				32MB
512K X 36-D	512K x 36-D	4M x 36-S	4M x 36-S	36MB
1M x 36-S	4M x 36-S	4M x 36-S		36MB
1M x 36-S	8M x 36-D			36MB
1M x 36-S	1M x 36-S	4M x 36-S	4M x 36-S	40MB
1M x 36-S	1M x 36-D	8M x 36-D'		40MB
4M x 36-S	4M x 36-S	4M x 36-S		48MB
4M x 36-S	8M x 36-D			48MB
4M x 36-S	4M x 36-S	4M x 36-S	4M x 36-S	64MB
4M x 36-S	4M x 36-S	8M x 36-D		64MB
1M x 36-S	16M x 36-S			68MB
16M x 36-S				64MB
8M x 36-D	8M x 36-D			64MB
256K x 36-S	16M x 36-S			65MB
1M x 36-S	8M x 36-D	8M x 36-D		68MB
1M x 36-S	1M x 36-D	8M x 36-D	8M x 36-D	72MB
1M x 36-S	1M x 36-S	16M x 36-S		72MB
4M x 36-S	16M x 36-S			80MB
4M x 36-S	8M x 36-D	8M x 36-D		80MB
4M x 36-S	4M x 36-S	8M x36-D	8M x 36-D	96MB
8M x 36-D	8M x 36-D	8M x 36-D		96MB
4M x 36-S	4M x 36-S	16M x 36-S		96MB
8M x 36-D	8M x 36-D	8M x 36-D	8M x 36-D	128MB
16M x 36-S	16M x 36-S			128MB

NOTE:
S = Single side, D = Double side.

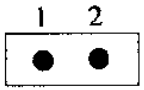
Green PC Function Support

Monitor Power Down Control

The connector JP38 support hardware method to control peripheral deivce. When power down, it will reduce power consumption. The JP38 are active after system "Doze Time" period.

The following is the application for the JP38.

For peripheral device using power supply AC output control pinout:



JP38

pin 1 : Control signal to power supply
pin 2 : Ground

Appendix A: System Layout